# METHOD FOR FORMING CONTACT

## FIELD OF INVENTION

The present invention relates to a method for forming contacts, and particularly, relates to a method for forming memory contacts on a semiconductor device.

## BACKGROUND OF THE INVENTION

Most integrated circuits are manufactured by repeating several semiconductor processes, e.g. photolithographing, etching, depositing and doping, and are accomplished with many layers. To transmit signals among those layers, contacts and conductive lines are indispensable to modern semiconductor processes, especially for manufacturing memory chips. The contacts in a memory at least include bit-line contacts and gate contacts, and their manufacturing quality has great effect upon functions of the memory.

FIGS. **1**~**4** show the steps for forming contacts on a semiconductor device in the prior art. The contacts are positioned on a substrate **102** which has a bit-line contact area **100** and a gate contact area **200**. FIG. **1**A shows the bit-line contact area **100** which includes a first polysilicon layer **104**, a conductive layer **106**, a first dielectric layer **108**, a side wall **110**, a second dielectric layer **112**, a third dielectric layer **114**, a fourth dielectric layer **116** and a second polysilicon layer **118**. FIG. **1**B shows the gate contact area **200** which includes a third polysilicon layer **204**, the conductive layer **106**, a fifth dielectric layer **208**, the fourth dielectric layer **116** and the second polysilicon layer **118**.

Referring to FIG. **1**A and FIG. **1**B, the method of the prior art coats a photoresist **120** on the bit-line contact area **100** as well as the gate contact area **200**, and then etches the two areas. Hence, a bit-line contact is formed on the bit-line contact area **100** as FIG. **2**A shows; however, a gate contact is not formed yet insofar as FIG. **2**B shows. The method of the prior art needs further steps of coating another photoresist **210** on the gate contact area **200**, as FIG. **3**A shows, and then etching the fifth dielectric layer **208** to form the gate contact as FIG. **3**B shows.

This kind of semiconductor process causes the aspect ratio too small to facilitate photoresist removal.

## SUMMARY OF THE INVENTION

The present invention provides a method for forming contacts on a semiconductor device, especially for forming memory contacts. The contacts mentioned herein are positioned on a substrate having a bit-line contact area and a gate contact area.

The method of the present invention includes the steps of forming an opening on the gate contact area, depositing a dielectric layer on the bit-line contact area and the opening, coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area, etching the dielectric layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening, removing the photoresist, and forming a conductive layer on the bit-line contact opening and the gate contact opening.

## BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1**A illustrates a sectional view of the bit-line contact area in the prior art;

FIG. **1**B illustrates a sectional view of the gate contact area in the prior art;



FIG. **2**A and FIG. **2**B illustrate sectional views for forming the bit-line contact opening in the prior art;

FIG. **3**A and FIG. **3**B illustrate sectional views for forming the gate contact opening in the prior art;

FIG. **4**A illustrates a sectional view of the bit-line contact area of the present invention;

FIG. **4**B illustrates a sectional view of the gate contact area of the present invention;

FIG. **5**A and FIG. **5**B illustrate sectional views for coating a photoresist to form an opening of the present invention;

FIG. **6**A and FIG. **6**B illustrate sectional views after the photoresist is removed;

FIG. **7**A and FIG. **7**B illustrate sectional views for depositing a dielectric layer;

FIG. **8**A and FIG. **8**B illustrate sectional views for coating another photoresist; and

FIG. **9**A and FIG. **9**B illustrate sectional views for forming the bit-line contact and the gate contact.

## DETAILED DESCRIPTION

FIGS. **4**~**9** show an embodiment of the present invention. FIG. **4**A shows the structure of a bit-line contact area **100** which includes a first polysilicon layer **104**, a conductive layer **106**, a first dielectric layer **108**, a side wall **110** and a second dielectric layer **112**. FIG. **4**B shows the structure of a gate contact area **200** which includes a third polysilicon layer **204**, the conductive layer **106** and a fifth dielectric layer **208**.

The method of the present invention includes the step of forming an opening on the gate contact area **200**. As FIG. **5**A and FIG. **5**B show, the method coats a photoresist **122** on the bit-line contact area **100** and the gate contact area **200** to define an opening pattern on the gate contact area **200** by means of the photolithography technique of the prior art. Next, the method etches the fifth dielectric layer **208** and then removes the photoresist **122**. As FIG. **6**A shows, the structure of the bit-line contact area **100** does not change, but as FIG. **6**B shows, the gate contact area **200** forms an opening **210**.

Then the method deposits a dielectric layer on the bit-line contact area **100** and the opening **210**. As FIG. **7**A and FIG. **7**B show, the dielectric layer includes a third dielectric layer **114** and a fourth dielectric layer **116**. In the embodiment, the third dielectric layer **114** is a borophospho-silicate glass (BPSG) layer. It is noted that an annealing process is preferably executed after the borophospho-silicate glass layer is deposited in order to reduce resistivity. The annealing temperature is 850~950° C. and the deposition depth of the borophospho-silicate glass layer on the bit-line contact area **100** after annealing is 2400~2500 Å. Moreover, the fourth dielectric layer **116** of the embodiment is a tetraethyl orthosilicate (TEOS) layer of a depth of 2600~4500 Å.

The method of the present invention further includes the step of forming a polysilicon layer **118** as a hard mask when etching the third dielectric layer **114** and the fourth dielectric layer **116**.

Referring to FIG. **8**A and FIG. **8**B, the method of the present invention coats another photoresist **124** to define a bit-line contact opening **126** on the bit-line contact area **100** and a gate contact opening **212** on the gate contact area **200**.

Then the third dielectric layer **114** and the fourth dielectric layer **116** is etched by using the photoresist as a mask to form the bit-line contact opening **126** and the gate contact opening **212**. Next, the method removes the photoresist **124** so that

the bit-line contact opening **126** and the gate contact opening **212** are accomplished as FIG. **9**A and FIG. **9**B show. Finally, a conductive layer is formed on the bit-line contact opening **126** and the gate contact opening **212** to be a medium for signal transmission.

The width W of the bit-line contact opening **126** made by the method of the present invention is 60~70 nm, which is 50~75% wider than that of the prior art. The larger aspect ratio facilitates photoresist removal.

The above description of the preferred embodiments is expected to clearly expound the characteristics of the present invention but not expected to restrict the scope of the present invention. Those skilled in the art will readily observe that numerous modifications and alteration of the apparatus may be made while retaining the teaching of the invention. Accordingly, the above disclosure should be construed as limited only by the bounds of the claims.

What is claimed is:

**1**. A method for forming a contact of a semiconductor device, the contact being positioned on a substrate, the substrate having a bit-line contact area and a gate contact area, the method comprising the steps of:

forming an opening on the gate contact area;

depositing a dielectric layer on the bit-line contact area and the opening;

coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area;

etching the dielectric layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening;

removing the photoresist; and

forming a conductive layer on the bit-line contact opening and the gate contact opening.

**2**. The method of claim **1**, wherein the depositing step further comprises:

depositing a borophospho-silicate glass (BPSG) layer;

annealing the borophospho-silicate glass layer, and

depositing a tetraethyl orthosilicate (TEOS) layer.

**3**. The method of claim **2**, wherein a deposition depth of the borophospho-silicate glass layer on the bit-line contact area after annealing is 2400~2500 Å.

**4**. The method of claim **2**, wherein a deposition depth of the tetraethyl orthosilicate layer is 2600~4500 Å.

**5**. The method of claim **2**, wherein a temperature for annealing the borophospho-silicate glass layer is 850~950° C.

**6**. The method of claim **1**, further comprising forming a polysilicon layer as a hard mask between the depositing step and the coating step.

**7**. A method for forming a contact of a semiconductor device, the contact being positioned on a substrate, the substrate having a bit-line contact area and a gate contact area, the method comprising the steps of:

forming an opening on the gate contact area;

depositing a borophospho-silicate glass (BPSG) layer on the bit-line contact area and the opening;

annealing the borophospho-silicate glass layer;

depositing a tetraethyl orthosilicate (TEOS) layer;

coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area;

etching the borophospho-silicate glass layer and the tetraethyl orthosilicate layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening;

removing the photoresist; and

forming a conductive layer on the bit-line contact opening and the gate contact opening.

**8**. The method of claim **7**, wherein a deposition depth of the borophospho-silicate glass layer on the bit-line contact area after annealing is 2400~2500 Å.

**9**. The method of claim **7**, wherein a deposition depth of the tetraethyl orthosilicate layer is 2600~4500 Å.

**10**. The method of claim **7**, wherein a temperature for annealing the borophospho-silicate glass layer is 850~950° C.

**11**. The method of claim **7**, further comprising forming a polysilicon layer as a hard mask between the step of depositing a tetraethyl orthosilicate layer and the coating step.

**12**. A method for forming a contact of a semiconductor device, the contact being positioned on a substrate, the substrate having a bit-line contact area and a gate contact area, the method comprising the steps of:

forming an opening on the gate contact area;

depositing a borophospho-silicate glass (BPSG) layer on the bit-line contact area and the opening;

annealing the borophospho-silicate glass layer under a temperature of 850~950° C.;

depositing a tetraethyl orthosilicate (TEOS) layer of a depth of 2600~4500 Å;

coating a photoresist to define a bit-line contact opening on the bit-line contact area and a gate contact opening on the gate contact area;

etching the borophospho-silicate glass layer and tile tetraethyl orthosilicate layer while using the photoresist as a mask to form the bit-line contact opening and the gate contact opening;

removing the photoresist; and

forming a conductive layer on the bit-line contact opening and the gate contact opening.

**13**. The method of claim **12**, wherein a deposition depth of the borophospho-silicate glass layer on the bit-line contact area after annealing is 2400~2500 Å.

**14**. The method of claim **12**, further comprising forming a polysilicon layer as a hard mask between the step of depositing a tetraethyl orthosilicate layer and the coating step.

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# EXHIBIT D

US006225187B1

(12) **United States Patent**
**Huang et al.**

(10) **Patent No.: US 6,225,187 B1**
(45) **Date of Patent: May 1, 2001**

(54) **METHOD FOR STI-TOP ROUNDING CONTROL**

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(73) Assignee: **Nanya Technology Corporation** (TW)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/283,301**

(22) Filed: **Apr. 1, 1999**

(30) **Foreign Application Priority Data**

Feb. 12, 1999 (TW) ..... 88102265

(51) **Int. Cl.**[7] ..... **H01L 21/76**
(52) **U.S. Cl.** ..... **438/424**; 438/431; 438/433
(58) **Field of Search** ..... 438/424, 435, 438/438, 692, 296, 431, 432, 433, 714

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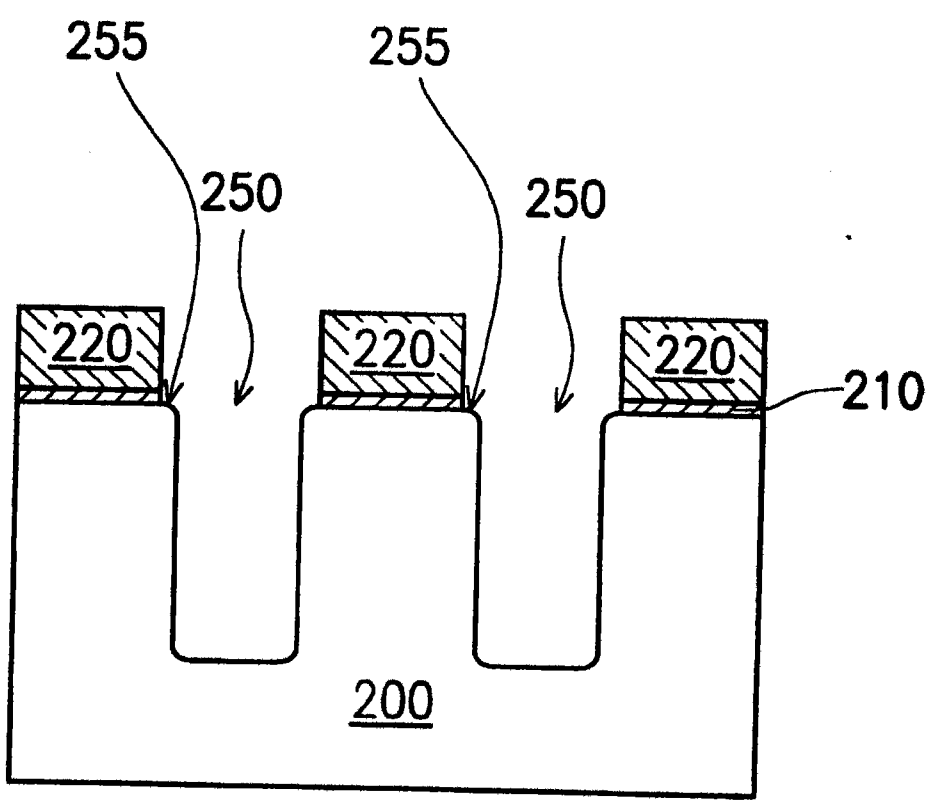
*Primary Examiner*—David Nelms
*Assistant Examiner*—Phuc T. Dang
(74) *Attorney, Agent, or Firm*—Michael D. Bednarek; Shaw Pittman

(57) **ABSTRACT**

This present discloses a method for STI top rounding control, the steps comprising: (a) providing a semiconductor substrate; (b) forming an oxide layer on the substrate; (c) forming a hard mask on the oxide layer; (d) forming a photoresist pattern with an opening exposing the hard mask at a predetermined STI trench region on the hard mask; (e) etching the exposed hard mask and the underlying oxide layer within the opening in sequence, and continuously over-etching to remove part of the semiconductor substrate to form a window lower than the surface of the oxide layer; and (f) using the photoresist pattern and the hard mask as an etching mask, removing part of the exposed semiconductor substrate in the window to form an STI trench.

**14 Claims, 4 Drawing Sheets**



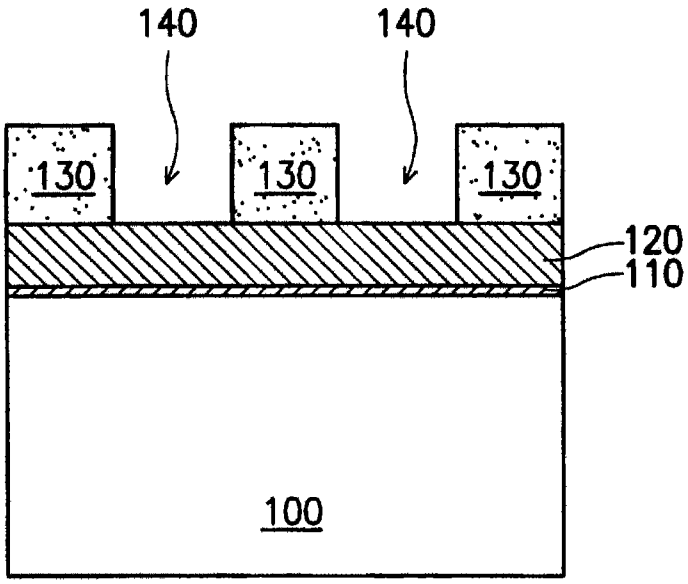

140
140
130
130
130
120
110
100

FIG. 1A

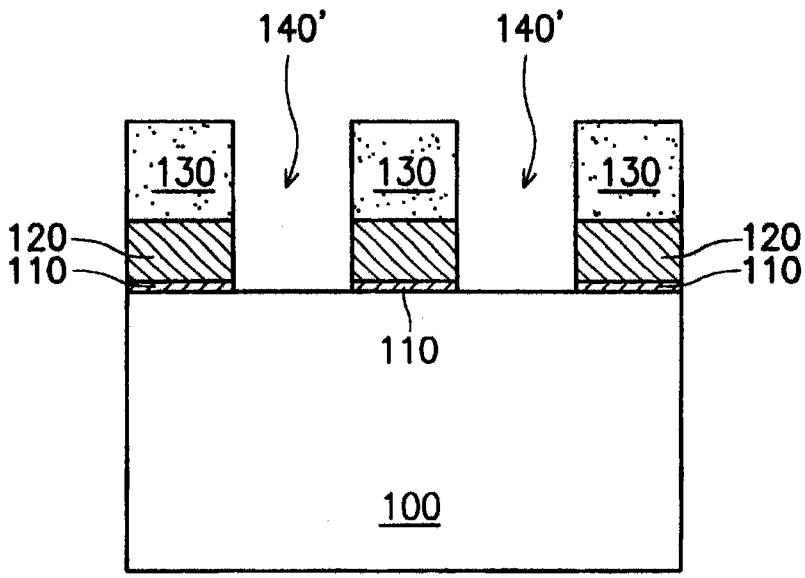

140'
140'
130
130
130
120
110
120
110
110
100

FIG. 1B

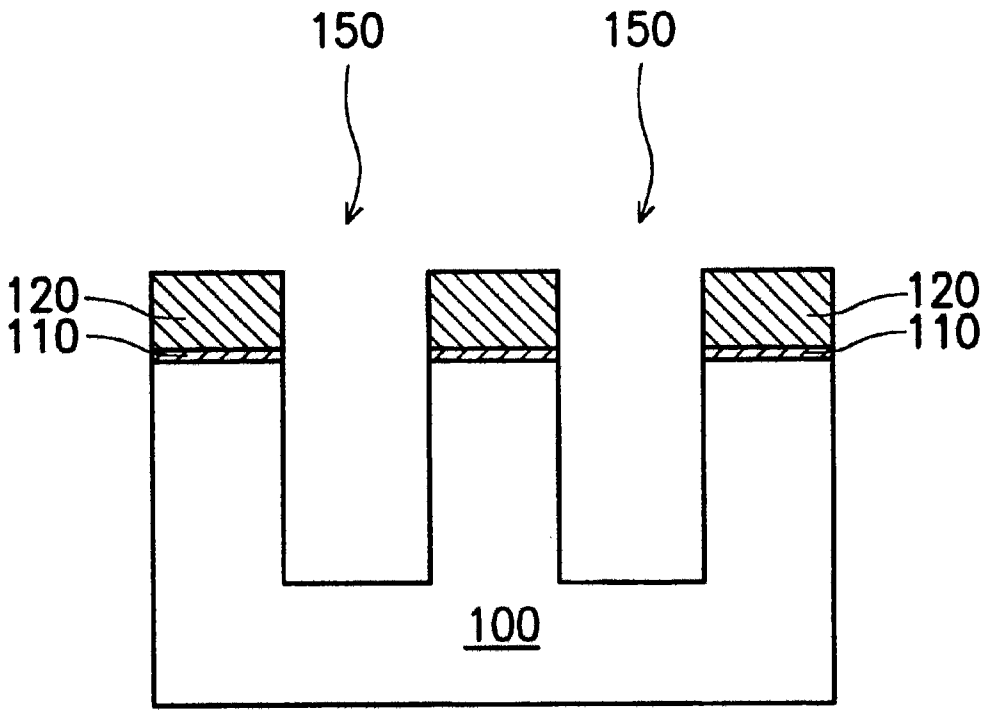



FIG. 1C

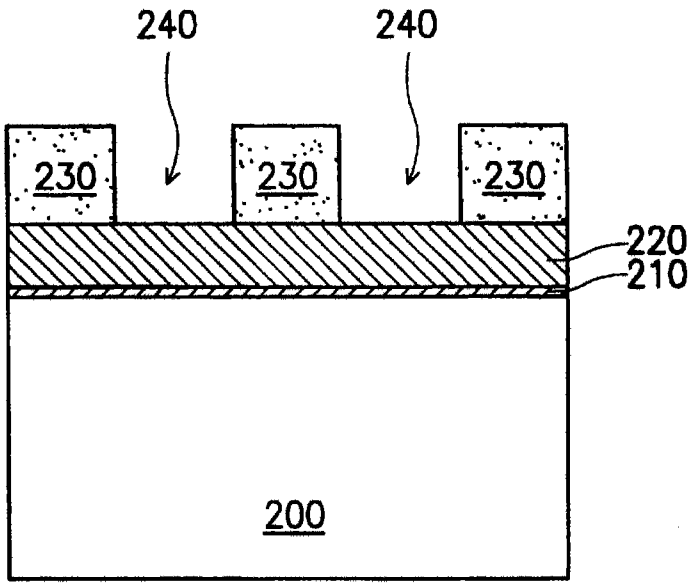

240
240
230
230
230
220
210
200

FIG. 2A

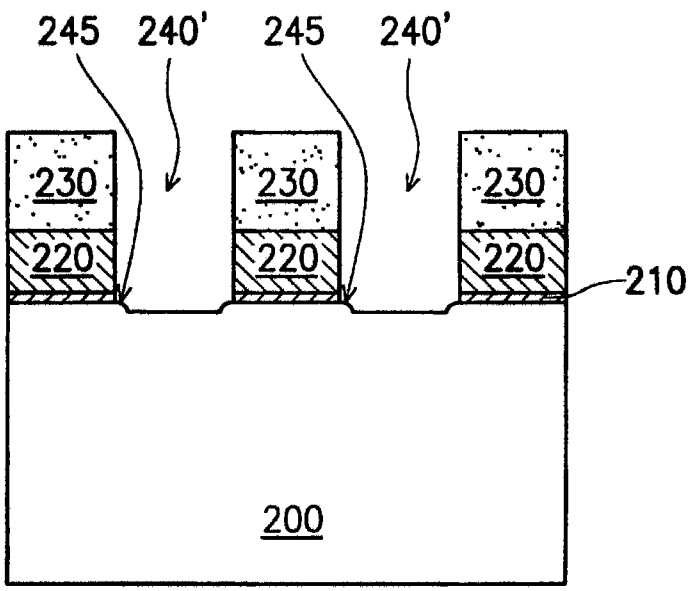

245
240'
245
240'
230
230
230
220
220
220
210
200

FIG. 2B

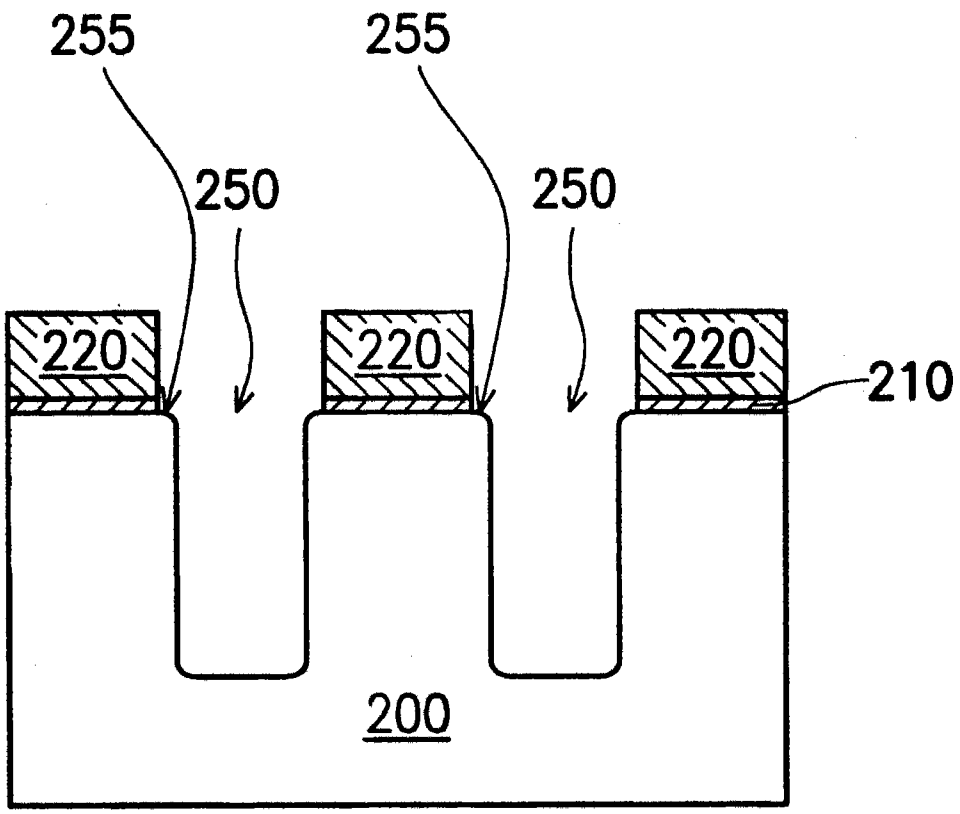



FIG. 2C

# METHOD FOR STI-TOP ROUNDING CONTROL

## FIELD OF THE INVENTION

The invention relates to an STI process, and more particularly relates to an STI top-rounding process.

## BACKGROUND OF THE INVENTION

With the increasing integration of ICs, hundreds of thousands of MOS transistors can be formed on a silicon substrate with an area of 1~2 $cm^2$ in an advanced VLSI process. In order to operate the transistors independently, each transistor must be isolated to prevent shorting. The process is called the "isolation process".

A conventional isolation process comprises the following steps. First, an oxide and a hard mask are formed on a semiconductor substrate in sequence. Then, a window is defined at the determined STI site by using photolithography and etching techniques. Subsequently, the exposed substrate within the window is removed to form an STI trench. The detailed process is illustrated in FIGS. 1A~1C.

First, referring to FIG. 1A, a semiconductor substrate **100**, such as a silicon substrate, is provided. Then, an oxide **110** (e.g. a silicon dioxide layer) and a hard mask layer **120** (e.g. a nitride layer) are formed on the semiconductor substrate **100** in sequence. Then, a photoresist pattern **130** with a opening **140** exposing the hard mask **120** at in a predetermined STI site is formed on the hard mask **120** by photolithography techniques.

Next, referring to FIG. 1B, the exposed hard mask **120** and the underlying oxide layer **110** and semiconductor substrate **100** within the opening **140** are etched to form an etching window **140'** exposing the semiconductor substrate **100** by means of photolithography techniques.

Finally, referring to FIG. 1C, the photoresist layer **130** is removed, and the exposed semiconductor substrate **100** within the opening **140'** is etched out by using the hard mask **120** as an etching mask, thus an STI trench **150** is formed. The STI trench **150** can be further gap-filled by an insulating material, though this step is not detailed here.

It is noted that the corners of the STI trench **150** are very sharp, therefore the STI channel obtained after gap-filling with an insulating material will make the insulating layer around the corners thinner than at other sites. Hence, leakage current or double hump may be apparent during operation, thus establishing a parasitic electric field.

In order to address the drawback of the conventional STI process described above, it is necessary to develop a novel STI process to forming top-rounded trenches for isolation.

## SUMMARY OF THE INVENTION

In order to address the drawback of the conventional STI process described above, this invention discloses a method for STI top-rounding control.

The feature of the invention is to provide a method for STI top rounding control, the steps comprising: (a) providing a semiconductor substrate; (b) forming an oxide layer on the substrate; (c) forming a hard mask on the oxide layer; (d) forming a photoresist pattern with a opening exposing the hard mask at a predetermined STI trench region on the hard mask; (e) etching the exposed hard mask and the underlying oxide layer within the opening in sequence, and continuously over-etching to remove part of the semiconductor substrate to form a window lower than the surface of the oxide layer; and (f) using the photoresist pattern and the hard mask as etching masks, removing part of the exposed semiconductor substrate within the window to form an STI trench.



In the method described above, the semiconductor substrate is a silicon substrate. The oxide layer consists of a silicon dioxide layer. The hard mask can be nitride selected from the group consists of silicon nitride or silicon oxynitride. The etching process applied in step (e) is dry-etching, wherein the etchant is composed of a mixture of $CHF_3/CF_4/O_2/AR$ ($Ar/CHF_3$ ratio ranging from 3~6) or $SF_6/CHF_3$ (ratio ranging from 1~3). The thickness of the removed substrate is about 100~300 Å. The etching process applied in step (f) is dry-etching, wherein the etchant is composed of a mixture of $HBr/Cl_2/O_2$ ($HBr/Cl_2$ ratio ranging from 1~5). Moreover, the method described above can further comprise a step of gap-filling the STI trench with an insulating material to form an STI channel. The material used to gap-fill the STI trench can be, for example, silicon dioxide.

Other feature and advantages of the invention will be apparent from the following detailed description, and from the claims.

## BRIEF DESCRIPTION OF THE DRAWING:

FIGS. 1A~1C are cross-sectional views of a conventional process for making STI trenches.

FIGS. 2A~2C are cross-sectional views of process for making STI trenches according to an embodiment of this invention.

## DETAILED DESCRIPTION OF THE INVENTION

The present invention provides a novel method for STI top rounding control characterized by defining the STI trenches by means of a two-step etching process.

According to the present invention, a substrate is provided first, wherein the substrate can further comprise semiconductor devices. Next, an oxide layer, for example a silicon dioxide layer, and a hard mask consisting of a nitride selected from silicon nitride or silicon oxynitride are formed on the semiconductor substrate in sequence. Subsequently, a photoresist pattern with an opening exposing the hard mask at a predetermined STI site is formed on the hard mask by means of photolithography.

Using the photoresist pattern as a mask, the exposed hard mask and the underlying oxide layer and part of the substrate are removed by means of dry etching to form a window lower than the surface of the oxide layer, wherein the etchant used in this dry-etching process is a mixture consisted of $CHF_3/CF_4/O_2/Ar$ or $SF_6/CHF_3$.

Then, using the photoresist pattern and the hard mask as an etching mask, the exposed semiconductor substrate within the window is etched-off by dry-etching to form an STI trench, wherein the etchant used in this dry-etching process is a mixture consisting of $HBr/Cl_2/O_2$.

Moreover, the method described above can further comprise a step of gap-filling the STI trench with an insulating material to form an STI channel.

Therefore, top-rounded STI trenches and/or channels can be obtained by using of this present invention, and leakage-current or double hump present in conventional STI process can be significantly reduced.

## EMBODIMENT OF THE INVENTION

First, referring to FIG. 2A, a semiconductor substrate **200** was provided. Then, an oxide layer **210** such as silicon

dioxide, and a hard mask **220** such as a nitride layer consisting of silicon nitride or silicon oxynitride were formed on the oxide layer **200** in sequence. Then, a photoresist pattern was formed on the hard mask **210** with an opening **240** exposing the hard mask **220** at the predetermined STI site by means of photolithography techniques.

Next, referring to FIG. **2B**, the exposed hard mask **220** and the underlying oxide layer **210** within the opening **240** were removed by an etching gas consisting of a mixture of $CHF_3/CF_4/O_2/Ar$ ($Ar/CHF_3$ ratio ranging from 3 to 6) or a mixture consisting of $SF_6/CHF_3$ (ratio ranging from 1~3) by using the photoresist pattern **230** as a mask. After the exposed hard mask **220** and the underlying oxide layer **210** were removed, part of the substrate with a thickness of 100~300 Å was removed by a subsequent over-etching process; thus, a windows **240'** with a surface lower than the oxide layer **210** was formed. It is noted that the corner **245** of the window **240'** was round.

Subsequently, referring to FIG. **2C**, the semiconductor substrate **200** within the window **240'** was removed by an etching gas consisting of a mixture of $HBr/Cl_2/O_2$ ($HBr/Cl_2$ ratio ranging from 1~5) using the photoresist pattern **230** and the hard mask **220** as an etching mask, thus forming an STI trench **250**. It is noted that because the corner **245** of the window **240'** was round, the corner **255** of the STI trench **250** was also round. Therefore, the method disclosed in this present invention is effective in addressing the drawback of the prior art. In addition, an insulating material can be used to gap-fill the STI trench **250** with round corners **255** to form an improved STI channel with round corners. Since this gap-filling step is not the feature of this invention, however, no detailed description will be given.

From the above description, one skilled in this art can easily ascertain the essential characteristics of the present invention, and, without departing from the spirit and scope thereof, can make various changes and modifications of the invention to adapt it to various usage and conditions. Thus, other embodiments also fall within the scope of the following claims.

What is claim:

**1**. A method for STI top-rounding control, the steps comprising:

(a) providing a semiconductor substrate;

(b) forming an oxide layer on the substrate;

(c) forming a hard mask on the oxide layer;

(d) forming a photoresist pattern with an opening exposing the hard mask at a predetermined STI trench region on the hard mask;

(e) etching the exposed hard mask and the underlying oxide layer within the opening in sequence, and continuously over-etching to remove part of the semiconductor substrate to form a window lower than the surface of the oxide layer wherein corners of the window are round; and

(f) using the photoresist pattern and the hard mask as an etching mask, removing part of the exposed semiconductor substrate within the window to form an STI trench.

**2**. The method as claimed in claim **1**, wherein the semiconductor substrate is a Si substrate.

**3**. The method as claimed in claim **1**, wherein the oxide consists of silicon dioxide.

**4**. The method as claimed in claim **1**, wherein the hard mask consists of nitride.

**5**. The method as claimed in claim **4**, wherein the hard mask consists of silicon nitride.

**6**. The method as claimed in claim **4**, wherein the hard mask consists of silicon oxynitride.

**7**. The method as claimed in claim **1**, wherein the step (e) is applied by means of dry-etching.

**8**. The method as claimed in claim **7**, wherein the etchant used in the etching step is a mixture consisting of $CHF_3/CF_4/O_2/Ar$.

**9**. The method as claimed in claim **7**, wherein the etchant used in the etching step is a mixture consisting of $SiF_6/CHF_3$.

**10**. The method as claimed in claim **1**, wherein the thickness of the semiconductor substrate removed during step (e) is about 100~300 Å.

**11**. The method as claimed in claim **1**, wherein step (f) is applied by means of dry-etching.

**12**. The method as claimed in claim **11**, wherein the etchant used in the etching step is a mixture consisting of $HBr/Cl_2/O_2$.

**13**. The method as claimed in claim **1**, further comprising a step of gap-filling the STI trench with an insulating material to form an STI channel.

**14**. The method as claimed in claim **13**, wherein the insulating material consists of silicon dioxide.

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# EXHIBIT E

US006426271B2

(12) **United States Patent**
**Chen et al.**

(10) **Patent No.: US 6,426,271 B2**
(45) **Date of Patent: Jul. 30, 2002**

(54) **METHOD OF ROUNDING THE CORNER OF A SHALLOW TRENCH ISOLATION REGION**

(75) Inventors: **Yi-Nan Chen**, Taipei; **Hsien-Wen Liu**, Tainan, both of (TW)

(73) Assignee: **Nanya Technology Corporation**, Taoyuan (TW)

( * ) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/790,493**

(22) Filed: **Feb. 23, 2001**

(30) **Foreign Application Priority Data**

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(51) **Int. Cl.**[7] ..... **H01L 21/76**
(52) **U.S. Cl.** ..... **438/435**; 438/424; 438/436; 438/437; 438/770
(58) **Field of Search** ..... 438/424, 435, 438/436, 437, 770

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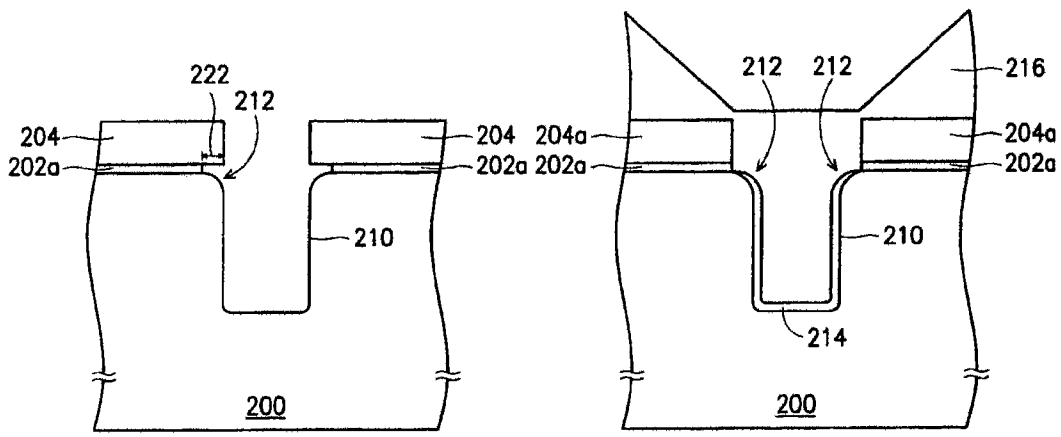
(74) *Attorney, Agent, or Firm*—Birch, Stewart, Kolasch & Birch, LLP

(57) **ABSTRACT**

The present invention provides a method of rounding the corner of the shallow trench isolation region, comprising the steps of: etching silicon substrate using a patterned mask layer and a pad oxide layer as an etch mask to form a trench in the silicon substrate, then removing part of the pad oxide layer, forming silicon dioxide on the surface of the silicon substrate in the trench, then removing part of the pad oxide layer and the silicon dioxide on the surface of the silicon substrate in the trench, repeating the step of oxidizing the surface of the silicon substrate and removing part of the pad oxide layer and silicon dioxide to round the corner of the trench, then performing the subsequent steps to form the shallow trench isolation region.

**20 Claims, 5 Drawing Sheets**



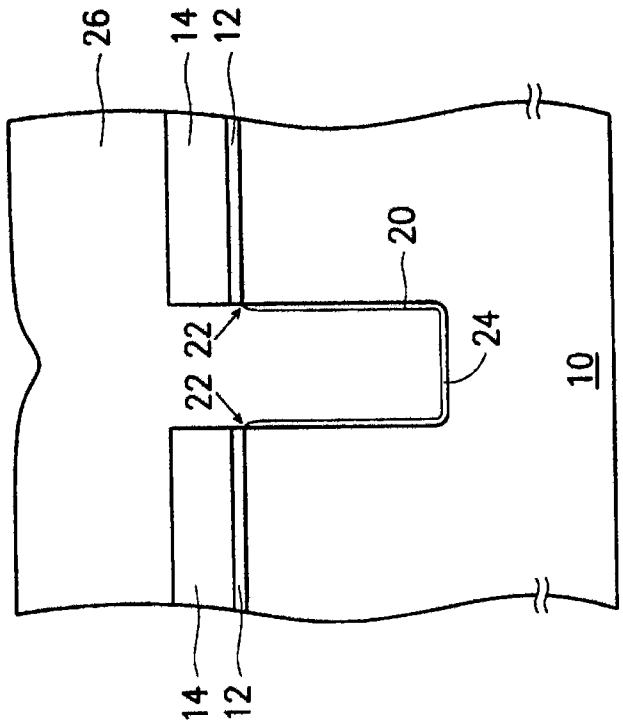



FIG. 1B
PRIOR ART

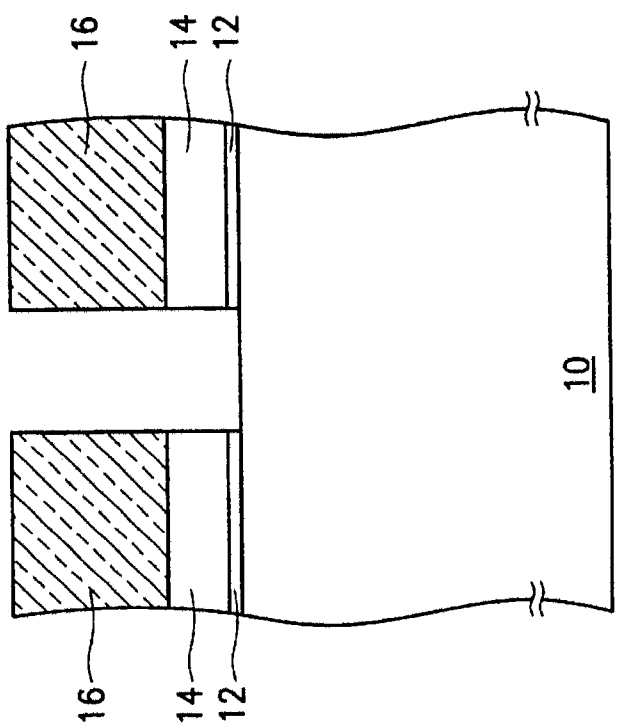



FIG. 1A
PRIOR ART

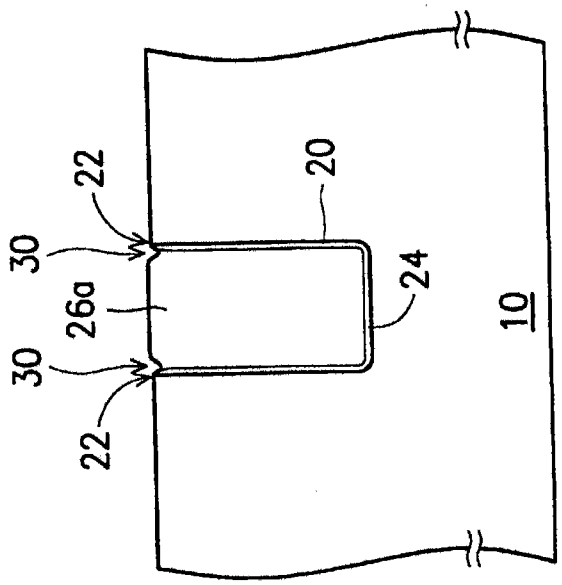



FIG. 1D
PRIOR ART

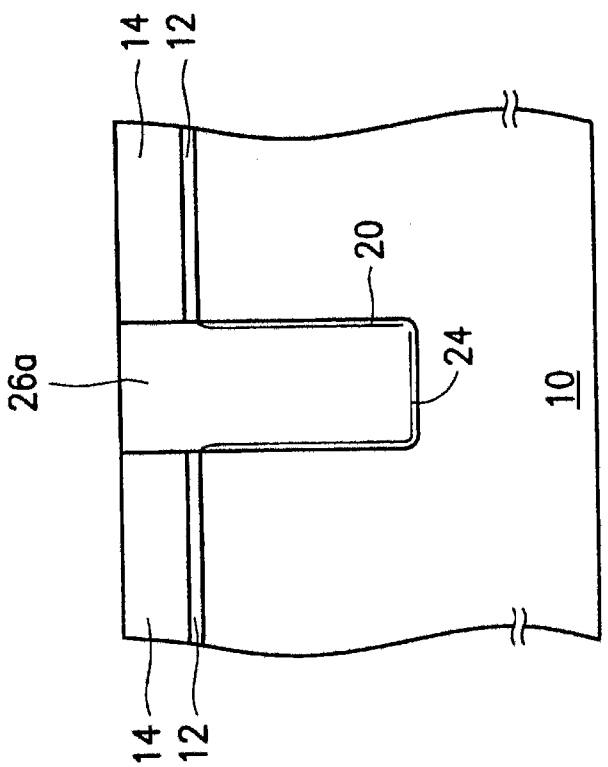



FIG. 1C
PRIOR ART

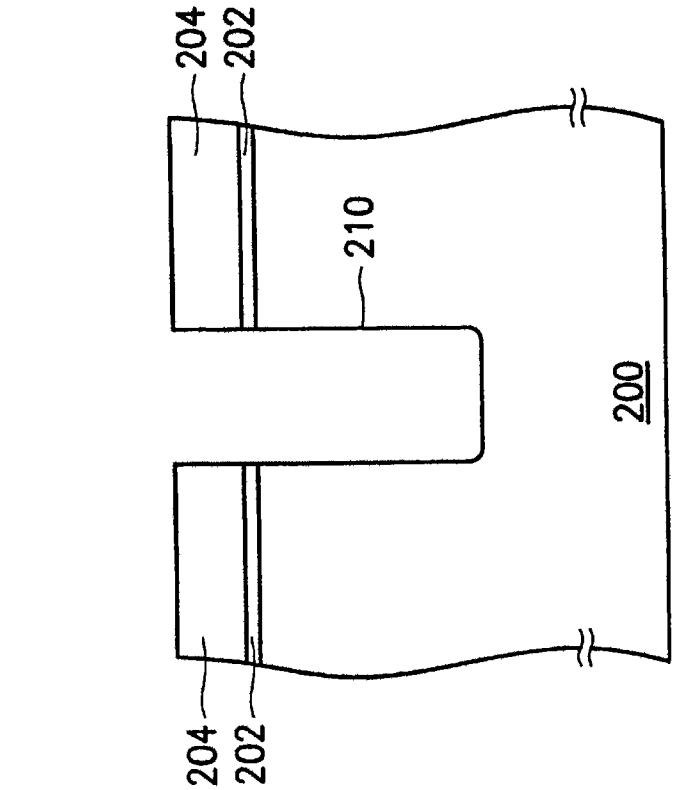



FIG. 2B

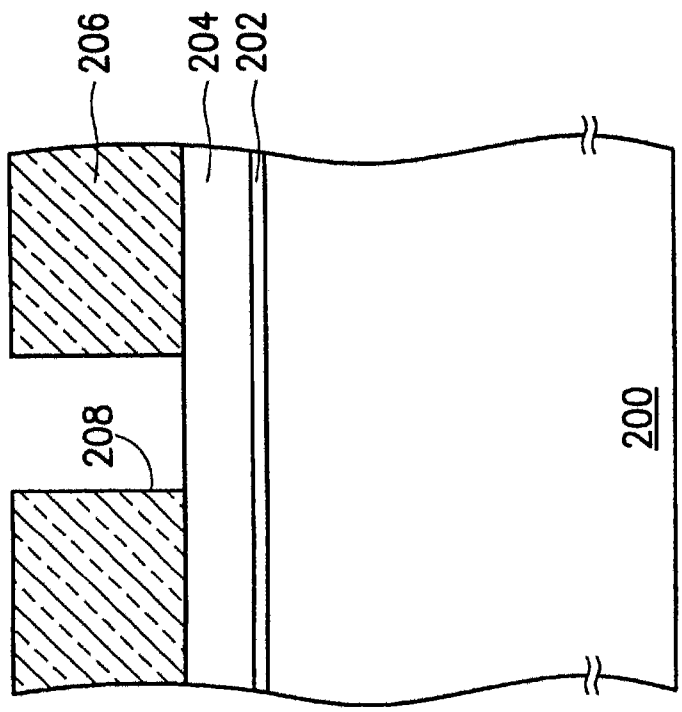



FIG. 2A

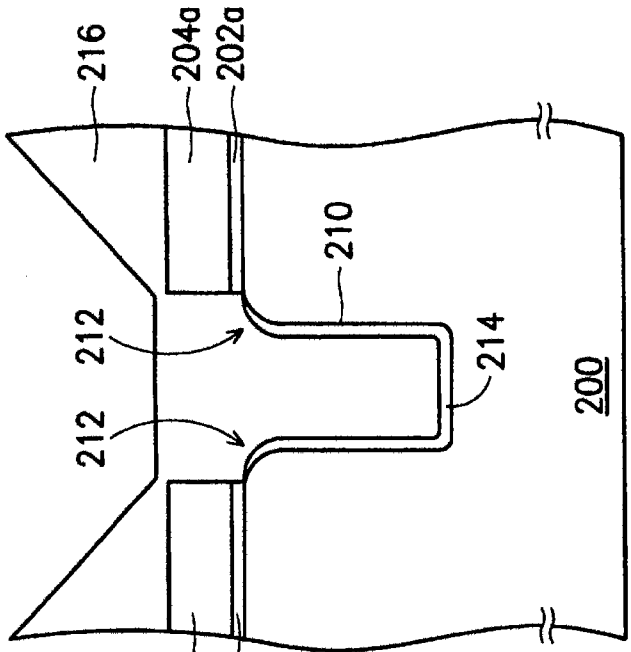
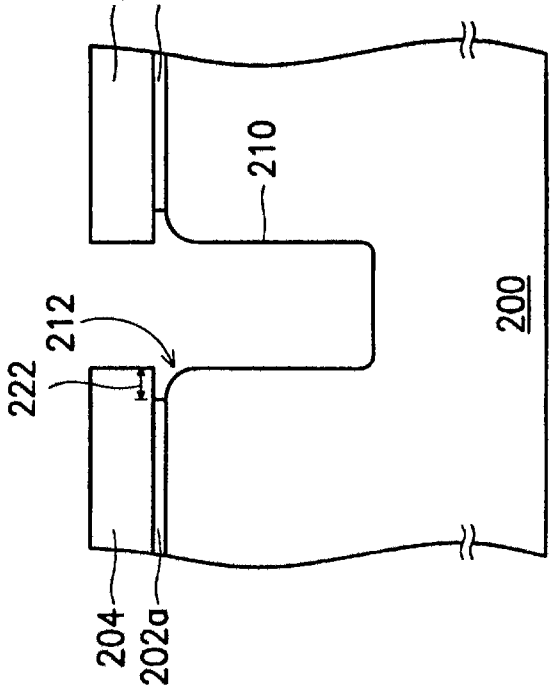

216
204a
202a
210
212
214
212
200
204a
202a

FIG. 2D


204
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210
212
222
200
204
202a

FIG. 2C

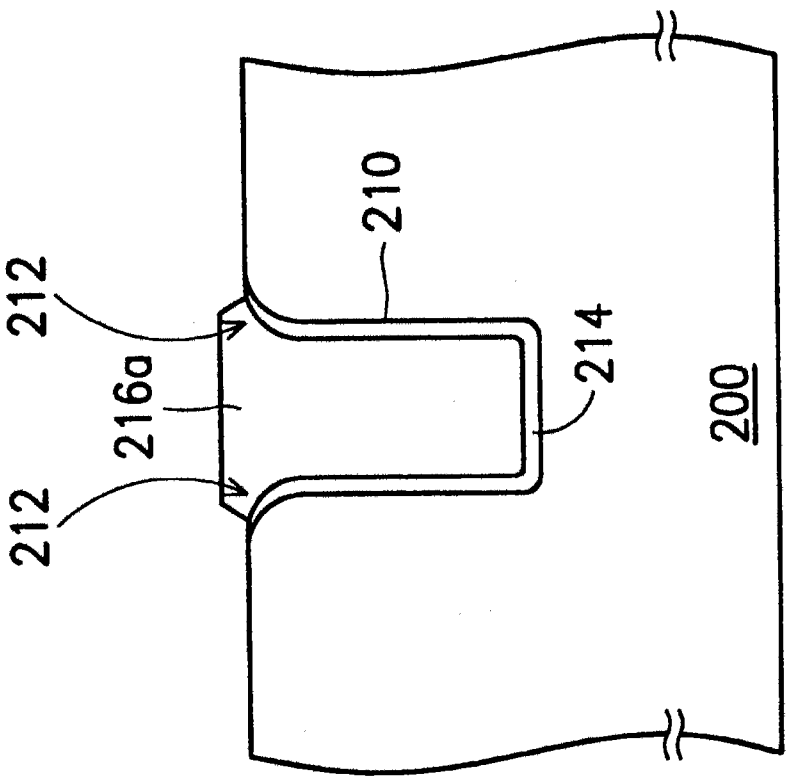



FIG. 2E

# METHOD OF ROUNDING THE CORNER OF A SHALLOW TRENCH ISOLATION REGION

## BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method of rounding the corner of shallow trench isolation region, more particularly to a chemical method of rounding the corner of the shallow trench isolation region.

2. Description of the Prior Art

Recently, as the manufacturing techniques of semiconductor integrated circuits develop, the number of elements in a chip increases. The size of the element decreases as the degree of integration increases. The line width used in manufacturing lines has decreased from sub-micron to quarter-micron, or even to a smaller size. However regardless of the reduction of the size of the element, adequate insulation or isolation must be formed among individual elements in the chip so that good element characteristics can be achieved. This technique is called device isolation technology. The main object is to form an isolation region, and reduce the size of the isolation to as small as possible while assuring good isolation effect to have larger chip space for more elements.

Among different element isolation techniques, LOCOS and shallow trench isolation region manufacturing methods are the two most used methods. In particular, as the latter has the small isolation region and can maintain the substrate to be level after the process is finished, it is the semiconductor manufacturing method obtaining the most attention.

The conventional manufacturing method for shallow trench isolation region is shown in the cross sectional views of FIGS. 1A to 1D.

Refer to FIG. 1A. A pad oxide layer **12** is formed on a silicon substrate **10** using thermal oxidation and a silicon nitride layer **14** is deposited on the pad oxide layer **12** using the CVD method. Next, a photoresist layer **16** is coated on the silicon nitride layer **14** and is patterned using photolithography to expose the portion where the element isolation region is to be formed. Silicon nitride layer **14** and pad oxide layer **12** are etched sequentially using the photoresist layer **16** as a mask.

Next, refer to FIG. **1B**, after photoresist layer **16** is removed with adequate liquid, silicon nitride layer **14** and pad oxide layer **12** are used as a mask to etch silicon substrate **10** to form trench **20** inside to define the active region of the element. Subsequently, thermal oxidation is performed to grow a thin silicon oxide layer as the lining oxide layer **24** on the bottom and sidewall of the trench **20**. However, when silicon oxide is formed, the stress is concentrated on the curvature region of a smaller radius, and the corner **22** of trench **20** is a sharp curvature of small radius, the growing speed of the silicon oxide at the corner **22** of the trench **20** is slower, so that the lining oxide layer **24** at the corner **22** of the trench **20** is very thin.

Next, chemical vapor deposition is performed, for example using $O_3$ and TEOS as a reactant to form oxide layer **26**, and fill the trench **20** and cover the surface of the silicon nitride layer **14**.

Next, refer to FIG. 1C. A chemical mechanical polishing process is performed, the part of oxide layer **26** that is higher than the surface of the silicon nitride layer **14** is removed to form the isolation region **26*a*** with a level surface. Subsequently, a suitable etching method is used to remove the silicon nitride layer **14** and pad oxide layer **12** in order



to complete the manufacturing of the shallow trench isolation, and obtain the structure shown in FIG. 1D.

Because the property of the element isolation region **26*a*** is similar to that of the pad oxide layer **12**, when etching liquid is used to dip pad oxide layer **12**, the element isolation region **26*a*** is inevitably etched so that the corner **22** of the trench **20** is exposed and an indentation **30** is formed next to the corner **22** of the trench **20**.

Thus, when the gate oxide layer and gate conductive layer are formed later, the conductive layer deposited in the indentation **30** is not easy to remove and a short circuit between the adjacent transistors is easily formed. In addition, since the gate oxide layer at the corner **22** of the trench **20** is thinner than other places, a parasitic transistor is formed. This phenomenon is equivalent to two transistors with gate oxide layers of different thickness in parallel. When current goes through this parasitic transistor, as the curvature radius of the corner **22** of the trench **20** is small, the electric fields concentrate and the Fowler-Nordheim current increases, hence the insulating property of the gate oxide layer of the corner **22** degrades, resulting in abnormal element characteristics. For example, there is a kink effect in I-V curvature of $I_d$ and $V_g$, which generates a double hump.

## SUMMARY OF THE INVENTION

From the above, the present invention provides a method of increasing the curvature radius of the corner of the trench.

Furthermore, the present invention provides a manufacturing method, which avoids forming a trench isolation region of parasitic transistors at the corner of the trench.

Furthermore, the present invention provides a manufacturing method of forming a trench isolation region, which avoids the short circuit that occurs between adjacent transistors.

Therefore, the present invention provides a method of rounding the corner of the shallow trench isolation region, the method includes: forming a pad oxide layer and mask layer sequentially on silicon substrate and patterning them, and then using the patterned pad oxide layer and mask layer as the etching mask to etch the silicon substrate and form the trench in the silicon substrate; next, use the oxidizing agent and HF liquid in turn to round the trench corner, subsequently remove part of the mask layer to expose the rounded corner of the trench, then forming an oxide layer to fill the trench, finally removing the mask layer and the pad oxide layer to form a trench isolation region.

According to one preferred embodiment of the present invention, the concentration of the HF liquid is about 0.3% to 2%. Oxidizing agents include $H_2O_{2(aq)}$ and $HNO_{3(aq)}$. The concentration of the $H_2O_{2(aq)}$ is about 5% to 20%; the concentration of the $HNO_{3(aq)}$ is about 3% to 30%. In the process of alternating use of the oxidizing agent and HF liquid, a de-ionizing water process, after the oxidizing agent and HF liquid process, is included.

The present invention provides a method of rounding the corner of the shallow trench isolation region, which includes the following steps: forming a pad oxide layer and a mask layer sequentially on a silicon substrate, and patterning them, then using patterned pad oxide layers and mask layers as etching masks to etch the silicon substrate and form a trench in the silicon substrate; next, after part of the pad oxide layer is removed, the surface of the silicon substrate in the trench is oxidized to form silicon dioxide, then part of pad oxide layer and silicon dioxide of the surface of the silicon substrate in the trench is removed, and repeating the step of oxidizing the surface of the silicon substrate and the

step of removing part of the pad oxide layer and silicon dioxide until the corner of the trench is rounded, then part of the mask layer is removed to expose the rounded corner of the trench, to form an oxide layer, filling the trench, finally removing the mask layer and the pad oxide layer to form the trench isolation region.

According to a preferred embodiment of the present invention, the method of oxidizing the silicon substrate includes using an oxidizing agent, this oxidizing agent includes $H_2O_{2(aq)}$ and $HNO_{3(aq)}$, after using this oxidizing agent, the method further includes a de-ionizing water process. The method of removing part of the pad oxide layer and silicon dioxide includes using HF liquid, after using this HF liquid, the method further includes a de-ionizing water process.

## BRIEF DESCRIPTION OF THE DRAWINGS

The following detailed description, given by way of example and not intended to limit the invention solely to the embodiments described herein, will best be understood in conjunction with the accompanying drawings, in which:

FIGS. 1A to 1D show the cross-sectional view of the manufacturing process of the conventional shallow trench isolation region;

FIGS. 2A to 2E show the cross sectional view of the process of the corner rounding of a shallow trench isolation region in accordance with a preferred embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

Embodiment:

FIGS. 2A to 2E show the cross sectional view of the process of corner rounding of a shallow trench isolation region in accordance with a preferred embodiment of the invention.

First refer to FIG. 2A. A semiconductor substrate, for example silicon substrate **200** is provided. A pad insulation layer (for example, pad oxide layer **202**) and a mask layer **204** are formed sequentially on the surface of the silicon substrate **200**. The method of forming the pad oxide layer **202** is thermal oxidation or chemical vapor deposition, in which the thermal oxidation is preferred. The mask layer is silicon nitride; its forming method is for example chemical vapor deposition. Next, a photoresist layer **206** is coated on the surface of the mask layer **204**, the photolithography is performed to define the photoresist pattern required to form opening **208**, the size of the opening is substantially the size of the element isolation region.

Next, refer to FIG. 2B. The patterned photoresist layer **206** is used as a mask to isotropicly etch the mask layer **204** and the pad oxide layer **202**, for example reactant ion etch process (RIE), to transfer the pattern of the photoresist layer **206** to mask layer **204** and the pad oxide layer **202**. Then, suitable liquid or dry etch process is performed to remove photoresist layer **206**.

Next, an isotropic etching process is performed using the mask layer **204** and pad oxide layer **202** as an etch mask, for example, the RIE process, etching silicon substrate **200** to a predetermined depth to form a trench **210** in the silicon substrate **200**.

Next, refer to FIG. 2C. A wet processing step is performed. This wet processing step includes using $HF_{(aq)}$ to remove part of the pad oxide layer **202**, then using an oxidizing agent to oxidize the surface of the silicon substrate **200** in the trench to form silicon dioxide ($SiO_2$) and using HF liquid to remove part of the pad oxide layer **202** and the formed silicon dioxide until the corner **212** of the trench **210** is rounded. At this time, the pad oxide layer **202** becomes a pad oxide layer **202***a* as shown; the length removed is about 130Å, i.e., the distance between the side of the mask layer **204** and the side of the pad oxide layer **202***a* is about 130Å.

In the above wet processing step, the concentration of the HF liquid is 0.3% to 2%. The oxidizing agent includes $H_2O_{2(aq)}$, $HNO_{3(aq)}$ or other liquids with similar properties. The concentration of $H_2O_{2(aq)}$ is about 5% to 20%; the concentration of $HNO_{3(aq)}$ is about 3% to 30%. This wet processing step can be performed by dipping or spreading.

In the above wet processing step, using $H_2O_{2(aq)}$ as the oxidizing agent, for example, when silicon substrate **200** is processed by $H_2O_{2(aq)}$, the following oxidation-reduction reaction occurs:

$$Si+2H_2O_2 \rightarrow SiO_2+2H_2O$$

When all Si on the surface of the silicon substrate **200** in the trench **210** is oxidized to become $SiO_2$, the reaction stops. Thus, the thickness of silicon lost is about 10 Å.

Subsequently, the following etch reaction occurs when $SiO_2$ is processed by $HF_{(aq)}$:

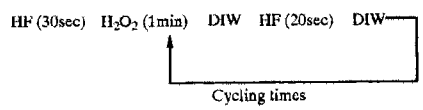
$$SiO_2+4HF \rightarrow SiF_{4(g)}+2H_2O$$

So that $SiO_2$ on the pad oxide layer **202** or the surface of the silicon substrate **200** in the trench **210** will react to form volatile $SiF_{4(g)}$.

It should be noted that the oxidizing agent and HF liquid cannot be used at the same time, or the reaction will get out of control.

Therefore, after silicon substrate is processed by oxidizing agent or HF liquid, it is washed using de-ionized water (DIW) to prevent unreacted oxidizing agents and HF liquid from being present at the same time or to prevent unreacted HF liquid and oxidizing agents from being present at the same time, to control more precisely the degree of the reaction.

To further elaborate this wet processing step, using the $H_2O_2$ as the oxidizing agent, and using dipping to perform set processing, the detailed process is as follows:




Wherein HF (30sec) means soaking for 30 seconds in HF liquid of 1% concentration for 30 seconds, HF (20 seconds) means soaking for 20 seconds, $H_2O_2$ (1 minute) means soaking $H_2O_2$ liquid of 35% concentration for 1 minute. Under this condition, the number of preferred cycling times is 5.

Next, referring to FIG. 2D, remove some of the mask layer **204** to rounded corner **212** of the exposed trench **210** to form the mask layer **204***a* as shown in the diagram, so that the subsequent oxides is easily filled into the trench **210**. The method of removing part of the mask **204**, for example, is soaking with hot $H_3PO_4$. Subsequently, a pad oxide layer **214** is formed on the surface of the silicon substrate **200** in the trench **210**, the method of forming may be for example, a rapid thermal oxidation process, the thickness of the formed pad oxide layer **214** is about 130 Å. Next, an insulating layer is formed above the mask layer **204***a*, for example, the oxide layer **216**, and fills the trench **210** and covers the rounded corner **212** of the trench **210**. The method of forming the oxide layer **216** uses high-density plasma deposition. Subsequently, an annealing process or rapid thermal process is performed to densitize the oxide layer **216**. The annealing process is performed for example, under a nitrogen atmosphere.

Next, refer to FIG. 2E, after removing the oxide layer **216** above the mask layer **204***a*, mask layer **204***a* and pad oxide layer **202***a* are removed sequentially to form the trench isolation region **216***a*. The method removing the oxide layer **216** above the mask layer **204***a* is for example, a chemical mechanical polishing method. The method of removing mask layer **204***a* is for example, soaking with hot $H_3PO_4$. The method of removing pad oxide layer **202***a* is for example, soaking with HF liquid. In addition, when removing pad oxide layer **202***a*, part of the oxide layer **216** will be removed at the same time. However, since the corner **212** of the trench **210** is rounded, the space blockage of the conducting material formed subsequent to the removing will not result, thus removing is easier to complete; Furthermore, the thickness of the gate oxide layer subsequently formed is more even. Also, because the curvature radius of the corner **212** of the trench **210** is larger, the electric fields are not concentrated at this region.

## THE FEATURE AND EFFECT OF THE INVENTION

From the above, the invention provides at least the following advantages:

1. The curvature radius of the corner of the trench of the present invention is larger than the corner of the trench formed in the shallow trench isolation region by the conventional manufacturing method.
2. Since the corner of the trench in the present invention is already rounded, the thickness of the gate oxide layer subsequently formed in this region is the same as in the other regions, thus no parasitic transistors will form and hence the problems that evolved with the parasitic transistors will not occur.
3. Since the corner of the trench of the present invention is already rounded, the conductive material subsequently formed in this region has no space blockage and is easily removed, thus preventing the short circuit between the adjacent transistors. Therefore, the shallow trench isolation region of the invention has good electrical insulation.

While the invention has been described by way of example and in terms of the preferred embodiment, it is to be understood that the invention is not limited to the disclosed embodiments. On the contrary, it is intended to cover various modifications and similar arrangements as would be apparent to those skilled in the art. Therefore, the scope of the appended claims should be accorded the broadest interpretation so as to encompass all such modifications and similar arrangements.

What is claimed is:

**1**. A method of rounding the corner of a shallow trench isolation region, comprising:

forming a pad insulating layer and a mask layer on a semiconductor substrate sequentially;

patterning the pad insulating layer and the mask layer, and etching the semiconductor substrate using the patterned pad insulating layer and the mask layer as the etch mask to form a trench in the semiconductor substrate;

using the oxidizing agent and the hf liquid alternately to round the corner of the trench;

removing part of the mask layer to the rounded corner that exposes the trench;

forming an insulating layer, filling the trench and covering the rounded corner of the trench; and

removing the mask layer and the pad insulating layer to form the trench isolation region.

**2**. The method as claimed in claim **1**, wherein the concentration of the HF liquid in the wet processing step is 0.3% to 2%.

**3**. The method as claimed in claim **1**, wherein the oxidizing agent comprises $H_2O_2$ liquid.

**4**. The method as claimed in claim **3**, wherein the concentration of the $H_2O_2$ liquid is 5% to 20%.

**5**. The method as claimed in claim **1**, wherein the oxidizing agent comprises $HNO_3$ liquid.

**6**. The method as claimed in claim **5**, wherein the concentration of the $HNO_3$ liquid is 3% to 30%.

**7**. The method as claimed in claim **1**, wherein during the process of alternately using the oxidizing agent and HF liquid, further comprising de-ionized water process after the HF liquid process.

**8**. The method as claimed in claim **1**, wherein during the process of alternately using the oxidizing agent and HF liquid, further comprising de-ionized water process after the oxidizing agent process and the HF liquid process.

**9**. The method as claimed in claim **1**, wherein before the process of alternately using the oxidizing agent and HF liquid, further comprising HF liquid process.

**10**. The method as claimed in claim **1**, wherein before the insulating layer is formed, further comprising forming a lining oxide layer on the surface of the semiconductor substrate in the trench.

**11**. A method of rounding the corner of a shallow trench isolation region, comprising the following steps:

(a) forming a pad oxide layer and a mask layer on the silicon substrate sequentially;

(b) patterning the pad oxide layer and the mask layer and etching the silicon substrate using the patterned pad oxide layer and mask layer as an etch mask to form a trench in the silicon substrate;

(c) removing part of the pad oxide layer;

(d) oxidizing the surface of the silicon substrate in the trench to form silicon dioxide;

(e) removing part of the pad oxide layer and silicon dioxide on the surface of the silicon substrate of the trench;

(f) repeating steps (d) and (e) until the corner of the trench is rounded;

(g) removing part of the mask layer to the rounded corner that exposes the trench;

(h) forming an oxide layer, filling the trench and covering the rounded corner of the trench; and

(i) removing the mask layer and the pad oxide layer to form the trench isolation region.

**12**. The method as claimed in claim **11**, wherein in the step (d) of forming silicon dioxide on the surface of the silicon substrate in the trench, an oxidizing agent is used.

**13**. The method as claimed in claim **12**, wherein after the process of using the oxidizing agent, a de-ionized water process is used.

**14**. The method as claimed in claim **12**, where the oxidizing agent includes either the $H_2O_2$ liquid or the $HNO_3$ liquid.

**15**. The method as claimed in claim **14**, wherein the concentration of the $H_2O_2$ liquid is 5% to 20%.

**16**. The method as claimed in claim **14**, wherein the concentration of the $HNO_3$ liquid is 3% to 30%.

**17**. The method as claimed in claim **11**, wherein in the steps (c) and (e) of removing part of the pad oxide layer and silicon dioxide on the silicon substrate of the trench comprises using HF liquid.

**18**. The method as claimed in claim **17**, wherein after using HF liquid, a de-ionized water process is used.

**19**. The method as claimed in claim **17**, wherein the concentration of the HF liquid is 0.3% to 2%.

**20**. The method as claimed in claim **11**, wherein in step (f), further comprises repeating steps (d) and (e) five times.

* * * * *

# EXHIBIT F

# United States Patent [19]

**Takemae et al.**

[11] **Patent Number: 4,641,166**

[45] **Date of Patent: Feb. 3, 1987**


[54] **SEMICONDUCTOR MEMORY DEVICE HAVING STACKED CAPACITOR-TYPE MEMORY CELLS**


[75] Inventors: **Yoshihiro Takemae**, Tokyo; **Tomio Nakano**, Kawasaki; **Kimiaki Sato**, Tokyo, all of Japan

[73] Assignee: **Fujitsu Limited**, Kawasaki, Japan



[21] Appl. No.: **560,171**

[22] Filed: **Dec. 12, 1983**

[30] **Foreign Application Priority Data**

Dec. 20, 1982 [JP] Japan ..... 57-222079

[51] **Int. Cl.**[4] ..... **H01L 29/78**

[52] **U.S. Cl.** ..... **357/23.6**; 357/51; 357/54

[58] **Field of Search** ..... 357/23.6, 23.11, 51, 357/24, 54



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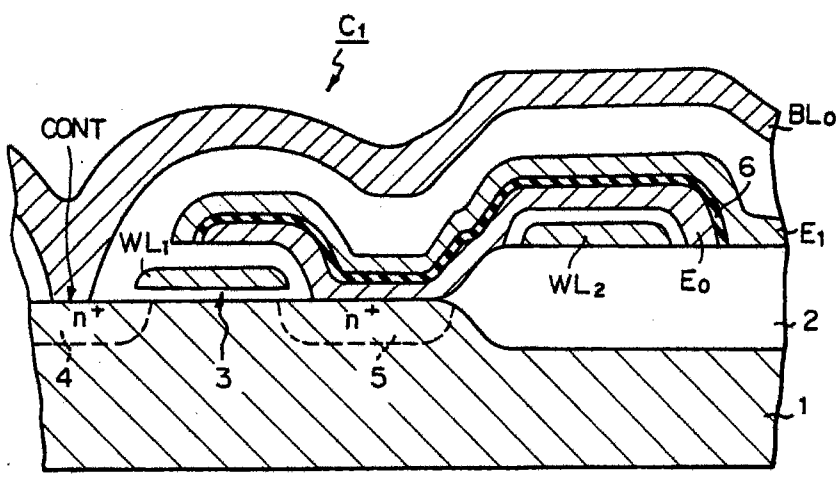
*Primary Examiner*—Martin H. Edlow
*Assistant Examiner*—Sara W. Crane
*Attorney, Agent, or Firm*—Staas & Halsey



[57] **ABSTRACT**

In a semiconductor memory device having stacked capacitor-type memory cells, the capacitor of each memory cell comprises an electrode, an insulating layer, and a counter electrode. The electrode is connected electrically to a source or drain region of a transfer transistor and extends over a part of a word line adjacent to another word line serving a gate electrode of the transfer transistor, at which part no memory cell is formed.


**10 Claims, 8 Drawing Figures**



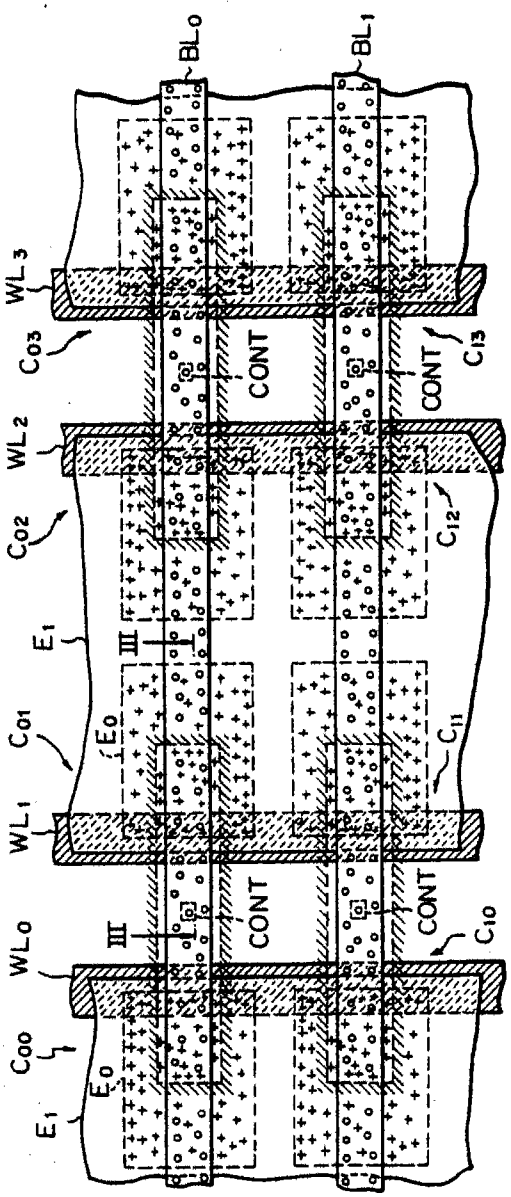



Fig. 1 PRIOR ART

Fig. 2 PRIOR ART

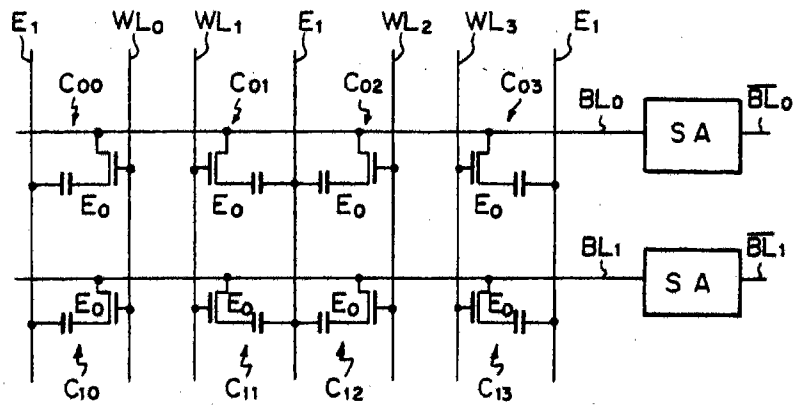
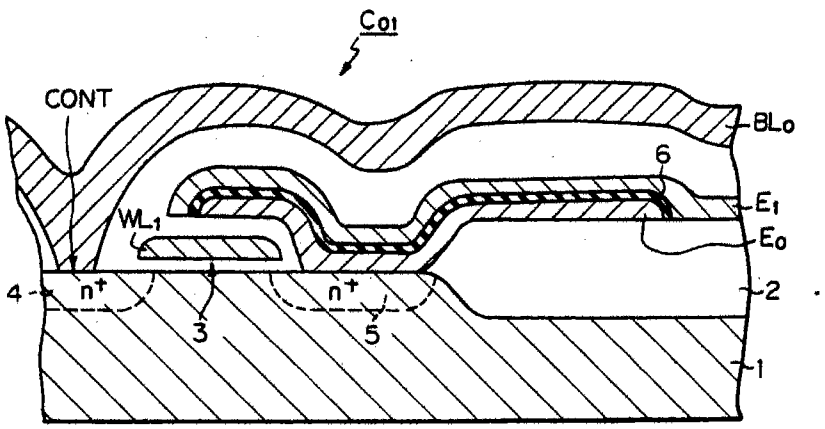
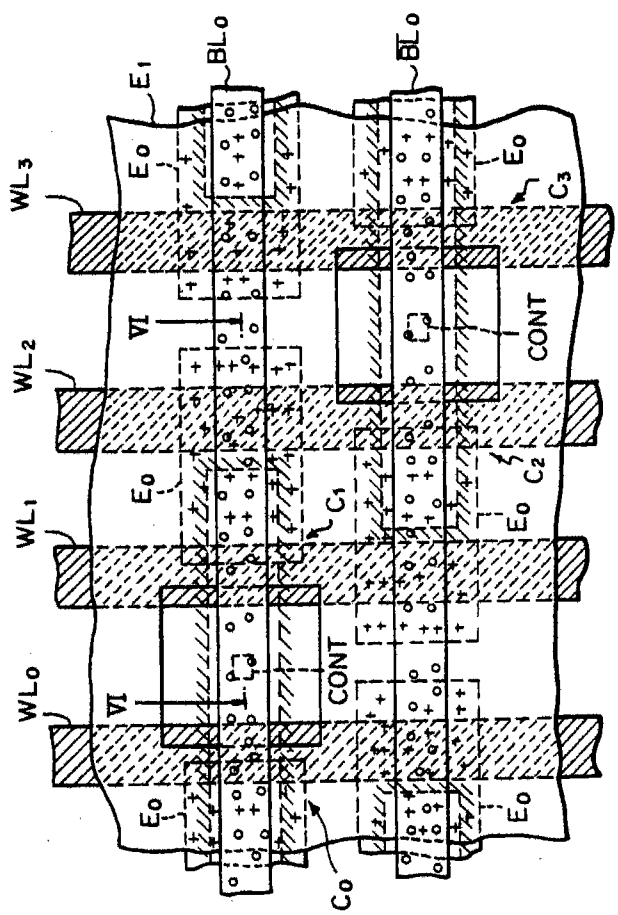



Fig. 3 PRIOR ART




BL0
BL0
E1
E0
E0
C3
WL3
VI
CONT
WL2
E0
C2
C1
E0
WL1
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WL0
VI
E0
E0
C0

Fig. 4

Fig. 5

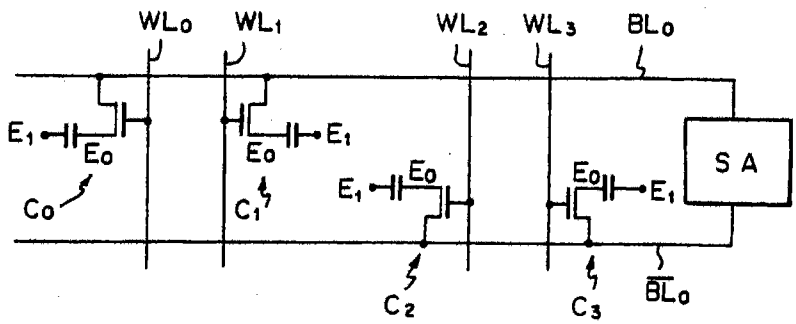
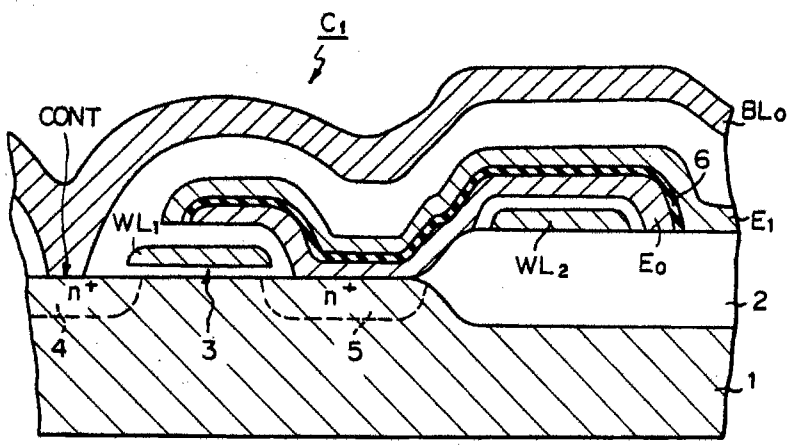

WL0
WL1
WL2
WL3
BL0
E1
E0
C0
C1
C2
C3
S A
BL0

Fig. 6


C1
CONT
BL0
6
WL1
E1
WL2
E0
n+
n+
2
4
3
5
1

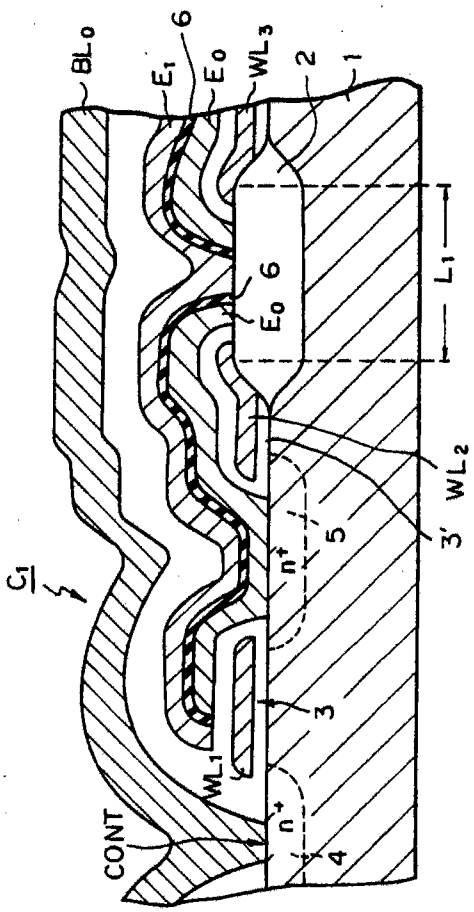
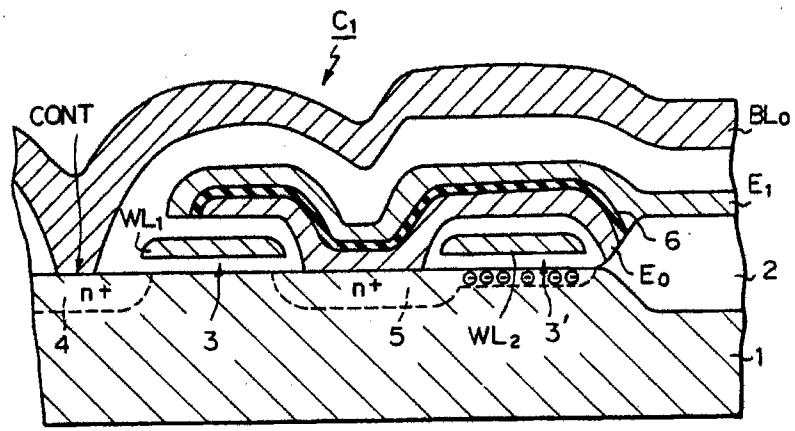



Fig. 7

Fig. 8



# SEMICONDUCTOR MEMORY DEVICE HAVING STACKED CAPACITOR-TYPE MEMORY CELLS

## BACKGROUND OF THE INVENTION

The present invention relates to a metal-oxide semiconductor (MOS, or, more broadly, MIS) dynamic semiconductor memory device having stacked capacitor-type memory cells.

Recently, MOS memory cells of a one-transistor one-capacitor type have usually been used in MOS dynamic memory devices. Fine lithographic technology has been developed so as to reduce the size of the elements of each memory cell, thereby obtaining a large capacity of a highly integrated semiconductor device. However, there is a limit to obtaining a high integration and a large capacity by size reduction only. In addition, size reduction of memory cells increases the generation rate of soft errors and the number of harmful effects due to hot electrons and hot holes. For improving memory cells of a one-transistor one-capacitor type, stacked capacitor-type memory cells have been proposed (see: Technical Digest of the Institute of Electronics and Communication Engineers of Japan, SSD80-30, 1980, July). Each stacked capacitor-type memory cell comprises a transfer transistor, which is the same as that of the conventional memory cell, and a capacitor which comprises an electrode extending over a thick field-insulating layer and over its own transfer transistor, a counter electrode disposed on the electrode, and an insulating layer therebetween, thereby increasing the capacitance of the capacitor.

In the prior art, however, such stacked capacitor-type memory cells have been applied to devices having "open bit lines" which are arranged on both sides of a series of sense amplifiers, not to devices having "folded bit lines" which are arranged on one side of a series of sense amplifiers.

## SUMMARY OF THE INVENTION

It is an object of the present invention to apply stacked capacitor-type memory cells to a semiconductor memory device having folded bit lines.

According to the present invention, the electrodes of a capacitor of a memory cell are formed on the part of an adjacent word line at which no memory cell is formed, thereby remarkably increasing the capacitance of the capacitor.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the description as set forth below with reference to the accompanying drawings.

FIG. 1 is a plan view of a prior art semiconductor memory device incorporating stacked capacitor-type memory cells.

FIG. 2 is an equivalent circuit diagram of the device of FIG. 1.

FIG. 3 is a cross-sectional view of the device of FIG. 1 taken along the line III—III in FIG. 1.

FIG. 4 is a plan view of an embodiment of the semiconductor memory device incorporating stacked capacitor-type memory cells according to the present invention.

FIG. 5 is an equivalent circuit diagram of the device of FIG. 4.



FIG. 6 is a cross-sectional view of the device of FIG. 4 taken along the line VI—VI in FIG. 4.

FIGS. 7 and 8 are modifications of the embodiment of FIG. 6.

## DESCRIPTION OF THE PREFERRED EMBODIMENTS

In FIG. 1, which illustrates the prior art, and in FIG. 2, which is an equivalent circuit diagram of the device of FIG. 1, stacked capacitor-type memory cells are provided at intersections between the word lines $WL_0$, $WL_1$, $WL_2$, and $WL_4$ and bit lines $BL_0$ and $BL_1$. A capacitor of each memory cell is comprised of an electrode $E_0$, a counter electrode $E_1$, and an insulating layer 6 (see FIG. 3) between the electrodes $E_0$ and $E_1$. Provided are the following conductive layers:

a first polycrystalline silicon layer for the word lines $WL_0$, $WL_1$, $WL_2$, and $WL_4$;

a second polycrystalline silicon layer for the electrode $E_0$;

a third polycrystalline silicon layer for the counter electrode $E_1$; and

an aluminum layer for the bit lines $BL_0$ and $BL_1$.

Note that "CONT" designates a contact hole for connecting the bit line $BL_0$ or $BL_1$ to an impurity diffusion (doped) region 4 on a semiconductor substrate 1 (see FIG. 3). In addition, the partly shaded areas designate field areas, and the inner areas thereof designate active areas.

One stacked capacitor-type memory cell, such as $C_{01}$, will be explained with reference to FIG. 3. In FIG. 3, a thick field oxide ($SiO_2$) layer 2 is formed on a $p^-$-type semiconductor substrate 1. Then a gate oxide ($SiO_2$) layer 3 is formed. Disposed on the layer 3 is a word line $WL_1$ serving as a gate of a transfer transistor which is made of the first polycrystalline silicon layer. After that, N+-type impurity diffusion regions 4 and 5 serving as a source and a drain, respectively, of the transfer transistor are formed by self-alignment.

An electrode $E_0$ made of the second polycrystalline silicon layer is formed on the word line $WL_1$ and the field oxide layer 2. In this case, the electrode $E_0$ is connected electrically to the impurity diffusion region 5. An insulating layer 6 as a capacitor dielectric, which is made of, for example, chemical vapor deposition (CVD) silicon nitride ($Si_3N_4$), is formed on the electrode $E_0$. Further, the counter electrode $E_1$ made of the third polycrystalline silicon layer is formed on the insulating layer 6.

Note that the insulating layer 6 has a large dielectric constant and a small leak current characteristic. The blank portions of FIG. 3 designate other insulating layers made of $SiO_2$, phosphosilicate glass (PSG), or the like.

In FIG. 3, since a capacitor formed by the electrode $E_0$, the insulating layer 6, and the counter electrode $E_1$ extends over the field oxide layer 2 and the word line $WL_1$, the capacitance thereof is larger than that of the conventional one-transistor one-capacitor type of memory cell in which a capacitor is formed on the impurity diffusion region 5. This characteristic is beneficial in obtaining a high integration and a large capacitance.

However, the stacked capacitor-type memory cells as illustrated in FIGS. 1 and 3 are applied to a device having an open bit line layout as illustrated in the equivalent circuit diagram of FIG. 2 but are not applied to a device having a folded bit line layout as illustrated in the equivalent circuit diagram of FIG. 5.

Note that the folded bit line layout, as compared with the open bit line layout, are disadvantageous in regard to integration density but are advantageous in regard to noise immunity since the noises generated in a pair of bit lines are compensated for by each other at a sense amplifier which senses and amplifies the potential difference between the bit line pair.

In FIG. 4, which illustrates an embodiment of the present invention, and in FIG. 5, which is an equivalent circuit diagram of the device of FIG. 4, stacked capacitor-type memory cells $C_0$ and $C_1$ are provided at intersections between the word lines $WL_0$ and $WL_1$ and the bit line $BL_0$, but no memory cells are provided at intersections between the word lines $WL_2$ and $WL_3$ and the bit line $BL_0$. On the other hand, stacked capacitor-type memory cells $C_2$ and $C_3$ are provided at intersections between the word lines $WL_2$ and $WL_3$ and the bit line $\overline{BL}_0$, but no memory cells are connected at intersections between the word lines $WL_0$ and $WL_1$ and the bit line $\overline{BL}_0$. That is, two memory cells are provided at every other intersection with the word line along one bit line. This is because a memory cell is connected at only one of the two intersections between each word line and each bit line pair, resulting in vacancy (i.e., nonconnection) at half of all the intersections, which tends to decrease the integration density of the device.

However, according to the present invention, the electrode $E_0$ of the capacitor of each memory cell is formed on its own word line (gate) and an adjacent word line to occupy the adjacent vacant intersection. In addition, the counter electrode $E_1$ of the capacitors of the memory cells is formed on the entire surface of the device except for contact areas including the contact holes CONT.

FIG. 6 is a cross-sectional view of the device of FIG. 4 taken along the line VI—VI in FIG. 4. In FIG. 6, the elements which are the same as those of FIG. 3 are denoted by the same reference numerals. As is illustrated in FIG. 6, the electrode $E_0$ made of the second polycrystalline silicon layer is provided over its own word line $WL_1$ (the first polycrystalline silicon layer) and the adjacent word line $WL_2$ (the first polycrystalline silicon layer). Thus, the capacitance of a capacitor formed by the electrode $E_0$, the counter electrode $E_1$, and the insulating layer 6 is increased, this being also beneficial in obtaining a high integration density and a large capacitance.

FIG. 7 is a modification of FIG. 6. The difference between FIG. 7 and FIG. 6 is that in FIG. 7 the word line $WL_2$ is disposed partly on the thick field oxide layer 2 and partly on the thin oxide layer 3', which is the same as the gate oxide layer 3. As a result, the width $L_1$ of the field oxide layer 2 can be almost a minimum line width determined by the manufacturing technology. In FIG. 7, since no field oxide layer 2 is present between the word lines $WL_1$ and $WL_2$, the connection area between the second polycrystalline silicon layer $E_0$ and the impurity diffusion region 5 is determined by the space between the word lines $WL_1$ and $WL_2$ only. Therefore, this space can be a minimum value. On the other hand, in FIG. 6, the above-mentioned connection area is determined by the word line $WL_1$ and the field oxide layer 2. Therefore, since this connection area is reduced due to the displacement of the alignment of the word line $WL_1$ and the field oxide layer 2, it is necessary to design the distance therebetween at a sufficient value. In addition, it is necessary to design the distance between the impurity diffusion region 5 and the word line $WL_2$ at a sufficient value in view of the displacement of the alignment therebetween. Thus, the space between the word lines $WL_1$ and $WL_2$ in FIG. 7 can be reduced as compared with that in FIG. 6.

FIG. 8 is also a modification of FIG. 6. The difference between FIG. 8 and FIG. 6 is that in FIG. 8 the insulating layer 3' immediately beneath the adjacent word line $WL_2$ is made thin. In this case, the insulating layer 3' is also the same as the gate oxide layer 3 immediately beneath the word line $WL_1$. For instance, it can be of silicon nitride. Further, N-type impurities are implanted in advance on the surface of the substrate 1 beneath the word line $WL_2$ by ion implantation or the like. Therefore, the MOS structure formed by the word line $WL_2$, the insulating layer 3', and the N-type impurity doped region of the substrate 1 serving as a charge-storing portion form a capacitor having a relatively large capacitance and which serves as a capacitor of the stacked capacitor-type memory cell (and has normally-on characteristics). As a result, the capacitance of the capacitor of the memory cell of FIG. 7 is increased as compared with that of FIG. 6.

Note that a $P^-$-type semiconductor substrate is used in the above-mentioned embodiments. However, obviously, a $N^-$-type substrate can be used.

As was explained hereinbefore, according to the present invention, the capacitor is formed on an adjacent word line so as to increase the capacitor capacitance, thereby obtaining a semiconductor memory device of a high integration density and a large capacitance having a folded bit line layout.

We claim:

1. A semiconductor memory device comprising:

a semiconductor substrate of a first conductivity type;

a plurality of word lines extending in parallel over said substrate;

a plurality of sense amplifiers;

a plurality of pairs of bit lines extending over said substrate transversely to said word lines, each said pair of bit lines being connected to corresponding inputs of a corresponding one of said sense amplifiers, and both of the bit lines of each said pair intersecting each of said word lines; and

stacked capacitor-type memory cells, each formed in the vicinity of an intersection between a corresponding one of said word lines and a corresponding one of said pairs of said bit lines,

wherein each of said memory cells comprises:

first and second impurity doped regions of a second conductivity type opposite to said first conductivity type formed in said substrate, each said first impurity doped region being electrically connected to a respective one of said bit lines, said first and second impurity doped regions and a respective portion of said corresponding one of said word lines forming a transfer transistor;

a first conductive layer electrically connected to said second impurity doped region, for forming a first of two capacitor electrodes, said first conductive layer extending over a respective part of another one of said word lines adjacent to said corresponding word line;

an insulating layer disposed on said first conductive layer; and

a second conductive layer, disposed on said insulating layer, for forming the second of said two capacitor electrodes.

2. A device as set forth in claim 1, wherein said first conductive layer of each said memory cell extends over a part of said corresponding word line of the memory cell.

3. A device as set forth in claim 1, further comprising a field insulating layer formed between said respective part of said another adjacent word line of each said memory cell and said substrate.

4. A device as set forth in claim 1 or 3, comprising a further insulating layer formed between said respective part of said another adjacent word line of each said memory cell and said substrate.

5. A device as set forth in claim 4, further comprising a third impurity doped region of said second conductivity type within said substrate beneath said respective part of said another adjacent word line and said further insulating layer of each said memory cell, so that a MIS structure formed by said respective part of said another adjacent word line, said further insulating layer, and said substrate has normally-on characteristics.



6. A device as set forth in claim 1, wherein said further insulating layer is made of silicon nitride.

7. The device of claim 4, further comprising a third impurity doped region of said second conductivity type within said substrate beneath said respective part of said another adjacent word line and said further insulating layer of each said memory cell, so that a MIS structure formed by said part of said another adjacent word line, said further insulating layer, and said substrate contribute to the capacitance of the memory cell.

8. The device of claim 1, 2, 3 or 6, wherein said device is of the folded-bit-line type.

9. The device of claim 8, wherein alternating ones of said word lines are effective for selecting a respective one of said memory cells of only a respective one of said bit lines of each said bit line pair.

10. The device of claim 8, wherein said first capacitor electrode is provided individually for each said memory cell, and said second capacitor electrode extends in common over all of said memory cells.

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